PowerNECS
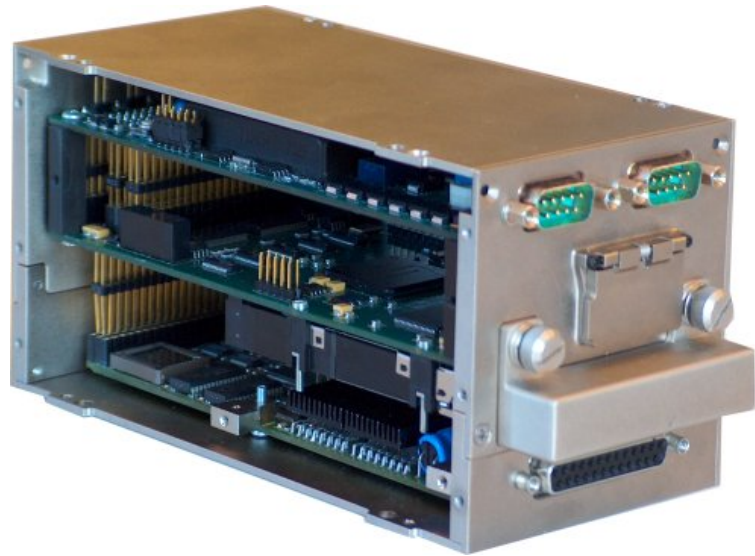
NECS system with PowerPC

PowerNECS is a NECS system with PowerPC Technology. The base unit consists of the power supply and the bus master module supporting one M-module that can be stacked on it. The master module is based on an MPC555 microcontroller operating at 40 MHz clock frequency and provides dual TPU and CAN interfaces, IrDA and two PCMCIA card slots. The bus master module also supports additional hardware, which can interface to the QSPIs (Queued Serial Peripheral Interface) and TPUs (Time Processor Unit) via a utility connector. The power supply module supplies the bus master module as well as all stacked-on modules with 5, 3.3 and +/- 12 VDC, which it derives from an unregulated EN2282 compliant power input. Additionally, it contains a four-character ASCII display for monitoring purposes. The power input lines are protected against polarity reversion, transient over voltage and electromagnetic interference. The PowerNECS runtime support and software library significantly reduce the time required for application software development. To maximize flexibility, application software can be downloaded, debugged and in-situ programmed on each PowerNECS unit via RS-232 using the Gnu gcc/gdb/XXgdb toolset or the eCOS real-time operating system.

Features:

> MPC555/40MHz microcontroller
> 2 MByte burst SRAM, 448 kByte internal flash
> 2 optically isolated CANbus interfaces according to ISO/DIS 11898
> M-Bus master interface for 1 M-module
> Ruggedized housing, EN2282 compliant power supply
> Programmable 4 character ASCII LED display
> Development support based on Gnu gcc/gdb/XXgdb and eCOS

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M-module Compliancy

* One M-module interfaces
* A08 D08/D16 address/data range
* INTA supported

PCMCIA / CANbus Compliancy

PCMCIA Compliancy
* Two type I or II, or one type III pc card slots
* Hot swap capability
* 3.3V or 5V support
CANbus Compliancy
* CAN protocol specification version 2.0
  ANB
* Optical isolation
* Programmable termination

Processor Configuration

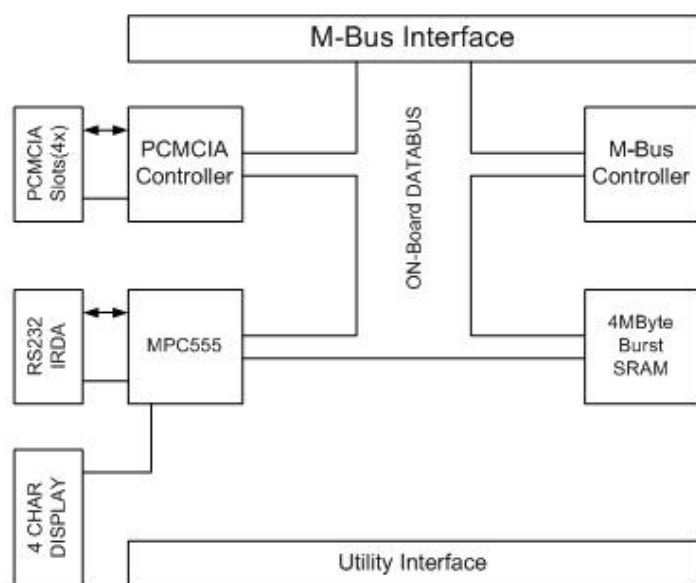* Motorola MPC555 Processor @40MHz
* 32-bit PowerPC architecture

Memory

* Up to 8 Mbyte of burst SRAM 32-bit wide
* 8 Kbyte SPI EEPROM
* 448 kByte Flash

Onboard resources

* Two TOUCAN CAN bus nodes
* IrDA interface
* Four character ASCII LED display
* Two PCMCIA slots

Ordering Information

* **PNECS** PowerNECS CPU unit
* **PNECSSupply** PowerNECS PowerSupply
  unit

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